Docket No.: 057454-0979 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Hideto HIDAKA	:	Confirmation Number: 7421
Application No.: 10/691,513 Patent No.: 6,987,690	:	Group Art Unit: 2827
Filed: October 24, 2003	:	Examiner: LE, THONG Q.

For: THIN FILM MAGNETIC MEMORY DEVICE FOR PROGRAMMING REQUIRED INFORMATION WITH AN ELEMENT SIMILAR TO A MEMORY CELL AND INFORMATION PROGRAMMING METHOD

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 CFR 1.322

Mail Stop COC
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reviewing the above-identified patent, a printing error was discovered therein requiring correction in order to conform the Official Record in the application.

The error noted is set forth on the two attached copies of form PTO-1050 Rev. 2-93 in the manner required by the Commissioner's Notice.

Specifically, One the title page of the Letters Patent, under section (56) References Cited, U.S. PATENT DOCUMENTS, **add** – 5,907,514 * 5/1999 Lee et al. –, Under section (56) References Cited, FOREIGN PATENT DOCUMENTS, **add**, -- WO 99/53499 10/1999 –, -- EP 1 132 924 A2 10/2000 –, and -- EP 1 253 651 A2 10/2002 –. Under section (56) References Cited, OTHER PUBLICATIONS, **change** " Durlam, M., et al. "Nonvolatile RAM based on magnetic tunnel junction elements" IEEE International Solid-State Circuits Conference, **February -9, 2000**, pp 130-131. " **to** -- Durlam, M., et al. "Nonvolatile RAM based on magnetic tunnel junction elements" IEEE

International Solid-State Circuits Conference, **February 7-9, 2000**, pp 130-131. – and **change** " Scheuerlein, R., et al. "A 10ns read and write non-volatile memory array using a magnetic **tunhnel** junction and FET switch in each cell" IEEE International Solid-State Circuits Conference, February 7-9, 2000, pp 128-129. " **to** -- Scheuerlein, R., et al. "A 10ns read and write non-volatile memory array using a magnetic **tunnel** junction and FET switch in each cell" IEEE International Solid-State Circuits Conference, February 7-9, 2000, pp 128-129. –. Under section (57) ABSTRACT, **change "24** Claims," to – **35** Claims, --. Under "What is Claimed is:", **add** claim 34 - 44 listed on the attached PTO 1050's. For your immediate reference attached is photocopies of PTO-892, Examiners initialed PTO-1449, the Amendment filed with the Request for Continued Examination dated January 7, 2005, the stamped returned postcard and Notice of Allowability with a mail date of March 9, 2005.

The change requested herein occurred as a result of printing the Letters Patent and the Certificate should be issued without expense under Rule 322 of the Rules of Practice. Accordingly, Applicants request issuance of the Certificate of Correction.

Please charge any shortage in fees due in connection with the filing of this paper to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Stephen A. Becker
Registration No. 26,527

Please recognize our Customer No. 20277 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 SAB:JGH
Facsimile: 202.756.8087
Date: October 27, 2006

Staple Here Only!

PRINTER'S TRIM LINE

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6987690

DATED : June 17, 2006

INVENTOR(S) : Hideto HIDAKA

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

One the title page of the Letters Patent,

Under section (56) References Cited, U.S. PATENT DOCUMENTS, **add** – 5,907,514 * 5/1999 Lee et al. –

Under section (56) References Cited, FOREIGN PATENT DOCUMENTS, **add**,
-- WO 99/53499 10/1999 –
-- EP 1 132 924 A2 10/2000 –
-- EP 1 253 651 A2 10/2002 –

Under section (56) References Cited, OTHER PUBLICATIONS,

Change " Durlam, M., et al. "Nonvolatile RAM based on magnetic tunnel junction elements" IEEE International Solid-State Circuits Conference, **February -9, 2000**, pp 130-131. " **to** -- Durlam, M., et al. "Nonvolatile RAM based on magnetic tunnel junction elements" IEEE International Solid-State Circuits Conference, **February 7-9, 2000**, pp 130-131. --

Change " Scheuerlein, R., et al. "A 10ns read and write non-volatile memory array using a magnetic **tunhnel** junction and FET switch in each cell" IEEE International Solid-State Circuits Conference, February 7-9, 2000, pp 128-129. " **to** -- Scheuerlein, R., et al. "A 10ns read and write non-volatile memory array using a magnetic **tunnel** junction and FET switch in each cell" IEEE International Solid-State Circuits Conference, February 7-9, 2000, pp 128-129. –

Under section (57) ABSTRACT, **change "24** Claims," to – **35** Claims, --

MAILING ADDRESS OF SENDER:
McDermott Will & Emery LLP
600 13th Street, NW
Washington, DC 20005
USA

PATENT NO.
6,987,690

No. of add'l copies
@ 50¢ per page

WDC99 1303243-1.057454.0979

OCT 3 1 2006

Staple Here Only!

PRINTER'S TRIM LINE

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6987690

DATED : June 17, 2006

INVENTOR(S) : Hideto HIDAKA

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Under "What is claimed is: ", add claim 34 – 44 as followed:

34. (Previously Presented) A thin film magnetic memory device, comprising:

a memory array having a plurality of memory cells arranged in a matrix, for magnetically storing data, wherein

each of said memory cells has a magnetic storage portion for storing

data when being magnetized in one of two directions,

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in at least one of data read operation and data write operation from and to said plurality of memory cells, wherein

said program circuit includes a plurality of program units for storing program data of said information when the program unit is in a program state,

each of said program units includes at least one program cell that is magnetized for data writing, and

a magnetization direction of each said magnetic storage portion in an initial state is the same as that of each said program cell in a non-program state.

MAILING ADDRESS OF SENDER:
McDermott Will & Emery LLP
600 13th Street, NW
Washington, DC 20005
USA

PATENT NO.
6,987,690

No. of add'l copies
@ 50¢ per page

WDC99 1303243-1.057454.0979

OCT 31 2006

Staple Here Only

PRINTER'S TRIM LINE

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6987690
DATED : June 17, 2006
INVENTOR(S) : Hideto HIDAKA

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Under "What is claimed is: ", add

35. (Previously Presented) A thin film magnetic memory device, comprising:

a memory array having a plurality of memory cells arranged in a matrix, for magnetically storing data, wherein

each of said memory cells has a magnetic storage portion for storing

data when being magnetized in one of two directions,

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in at least one of data read operation and data write operation from and to said plurality of memory cells, wherein

said program circuit includes a plurality of program units for storing program data of said information when the program unit is in a program state,

each of said program units includes at least one program cell that is magnetized for data writing, and wherein

the magnetization directions of each said magnetic storage portion and each said program cell are respectively set along an easy axis specific to said program cell, and

said magnetic storage portion and said program cell are arranged so that said respective easy axis thereof extend in a same direction.

MAILING ADDRESS OF SENDER:
McDermott Will & Emery LLP
600 13th Street, NW
Washington, DC 20005
USA

PATENT NO.
6,987,690

No. of add'l copies
@ 50¢ per page

FORM **PTO 1050** (Rev. 2-93)

OCT 31 2006

Staple Here Only!

PRINTER'S TRIM LINE

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6987690

DATED : June 17, 2006

INVENTOR(S) : Hideto HIDAKA

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Under "What is claimed is: ", add

36. (Previously Presented) A thin film magnetic memory device, comprising:

a memory array having a plurality of memory cells arranged in a matrix, for magnetically storing data, wherein

each of said memory cells has a magnetic storage portion for storing data when being magnetized in one of two directions,

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in at least one of data read operation and data write operation from and to said plurality of memory cells, wherein

said program circuit includes a plurality of program units for storing program data of said information when the program unit is in a program state,

each of said program units includes at least one program cell that is magnetized for data writing, and wherein

each said magnetic storage portion and each said program cell include

a first magnetic layer magnetized in a fixed direction,

a second magnetic layer magnetized either in a same direction as, or in an opposite direction to, that of said first magnetic layer depending on storage data, and

an insulating film formed between said first and second magnetic layers, and

in each said program cell in said non program state and each said magnetic storage portion in said initial state, said first and second magnetic layers are magnetized in a same direction.

MAILING ADDRESS OF SENDER:
McDermott Will & Emery LLP
600 13th Street, NW
Washington, DC 20005
USA

PATENT NO.
6,987,690

No. of add'l copies
@ 50¢ per page

FORM PTO 1050 (Rev. 2-93)

Staple Here Only!

PRINTER'S TRIM LINE

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6987690

DATED : June 17, 2006

INVENTOR(S) : Hideto HIDAKA

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Under "What is claimed is: ", add

37. (Previously Presented) The thin film magnetic memory device according to claim 36, wherein a step of magnetizing said magnetic storage portions to said initial state and a step of said magnetizing each program cells to said non-program state are conducted simultaneously.

38. (Previously Presented) A thin film magnetic memory device, comprising: a memory array having a plurality of memory cells arranged in a matrix, for magnetically storing data, wherein

each of said memory cells has a magnetic storage portion for storing data when being magnetized in one of two directions,

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in at least one of data read operation and data write operation from and to said plurality of memory cells, wherein

said program circuit includes a plurality of program units for storing program data of said information when the program unit is in a program state,

each of said program units includes at least one program cell that is magnetized for data writing, and wherein

said memory array further includes

redundant circuits provided respectively corresponding to prescribed blocks of said plurality of memory cells, each for replacing the prescribed block including a defective memory cell, and

said information stored in said program circuit includes a defective address for specifying the prescribed block including said defective memory cell,

said thin film magnetic memory device further comprising:

a redundant control circuit for controlling access to said redundant circuits based on a comparison result between an address signal for selecting said prescribed blocks and said defective address stored in said program circuit.

MAILING ADDRESS OF SENDER:
McDermott Will & Emery LLP
600 13th Street, NW
Washington, DC 20005
USA

PATENT NO.
6,987,690

No. of add'l copies
@ 50¢ per page

FORM PTO 1050 (Rev. 2-93)

OCT 3 1 2006

Staple Here Only!

PRINTER'S TRIM LINE

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6987690

DATED : June 17, 2006

INVENTOR(S) : Hideto HIDAKA

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Under "What is claimed is: ", add

39. (Previously Presented) The thin film magnetic memory device according to claim 38, wherein.

when said defective address is selected by said address signal, said redundant control circuit provides an instruction to access said redundant circuits and an instruction to discontinue access to a prescribed block corresponding to said address signal.

40. (Previously Presented) The thin film magnetic memory device according to claim 38, further comprising:

a monitor terminal for outputting an electric signal according to said comparison result in said redundant control circuit.

41. (Previously Presented) A thin film magnetic memory device, comprising: a memory array having a plurality of memory cells arranged in a matrix, for magnetically storing data, wherein

each of said memory cells has a magnetic storage portion for storing data when being magnetized in one of two directions,

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in at least one of data read operation and data write operation from and to said plurality of memory cells, wherein

said program circuit includes a plurality of program units for storing program data of said information when the program unit is in a program state,

each of said program units includes at least one program cell that is magnetized for data writing, and wherein

a bias voltage applied to each said program cell in program data read operation from said program cell is lower than a voltage applied to each said magnetic storage portion in normal data read operation.

MAILING ADDRESS OF SENDER:
McDermott Will & Emery LLP
600 13th Street, NW
Washington, DC 20005
USA

PATENT NO.
6,987,960

No. of add'l copies
@ 50¢ per page

FORM PTO 1050 (Rev. 2-93)

OCT 31 2006

Staple Here Only

PRINTER'S TRIM LINE

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6987690
DATED : June 17, 2006
INVENTOR(S) : Hideto HIDAKA

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Under "What is claimed is: ", add

42. (Previously Presented) A thin film magnetic memory device, comprising:

a memory array having a plurality of memory cells arranged in a matrix, for magnetically storing data, wherein

each of said memory cells has a magnetic storage portion for storing data when being magnetized in one of two directions,

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in at least one of

data read operation and data write operation from and to said plurality of

memory cells, wherein

said program circuit includes a plurality of program units for storing program data of said information when the program unit is in a program state,

each of said program units includes at least one program cell that is magnetized for data writing, and wherein

a period during which a bias voltage is applied to each said program cell in program data read operation from said program cell is shorter than that during which a voltage is applied to each said magnetic storage portion in normal data read operation.

MAILING ADDRESS OF SENDER:
McDermott Will & Emery LLP
600 13th Street, NW
Washington, DC 20005
USA

PATENT NO.
6,987,690

No. of add'l copies
@ 50¢ per page

FORM **PTO 1050** (Rev. 2-93)

OCT 31 2006

Staple Here Only!

PRINTER'S TRIM LINE

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6987690

DATED : June 17, 2006

INVENTOR(S) : Hideto HIDAKA

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Under "What is claimed is: ", add

43. (Previously Presented) A thin film magnetic memory device, comprising:

a memory array having a plurality of memory cells arranged in a matrix, for magnetically storing data, wherein

each of said memory cells has a magnetic storage portion for storing data when being magnetized in one of two directions,

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in at least one of data read operation and data write operation from and to said plurality of memory cells, wherein

said program circuit includes a plurality of program units for storing program data of said information when the program unit is in a program state,

each of said program units includes at least one program cell that is magnetized for data writing, and wherein

a voltage supplied to each said program cell in program data operation by a physical breakdown operation is higher than a voltage applied to each said magnetic storage portion in normal data read operation.

MAILING ADDRESS OF SENDER:
McDermott Will & Emery LLP
600 13th Street, NW
Washington, DC 20005
USA

PATENT NO.
6,987,690

No. of add'l copies
@ 50¢ per page

FORM **PTO 1050** (Rev. 2-93)

OCT 3 1 2006

Staple Here Only!

PRINTER'S TRIM LINE

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6987690
DATED : June 17, 2006
INVENTOR(S) : Hideto HIDAKA

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Under "What is claimed is: ", add

44. (New) A semiconductor memory device, comprising:

a first memory including normal memory cells for storing data therein;

an address decoder coupled to said first memory and selecting the normal memory cells according to the address provided to the semiconductor memory device; and

a redundant controller coupled to said address decoder and including a second memory for storing addresses of the defective normal memory cells of said first memory, wherein said second memory has a magneto-resistance element;

said semiconductor memory device further comprises

a third memory including spare memory cells for repairing the defective normal memory cells; and

a redundant address decoder coupled to said redundant controller and said third memory, and selecting the spare memory cells according to the address stored in said second memory.

MAILING ADDRESS OF SENDER:
McDermott Will & Emery LLP
600 13th Street, NW
Washington, DC 20005
USA

PATENT NO.
6,987,690

No. of add'l copies
@ 50¢ per page

FORM **PTO 1050** (Rev. 2-93)

OCT 31 2006

Notice of References Cited	Application/Control No. 10/691,513	Applicant(s)/Patent Under Reexamination HIDAKA, HIDETO	
	Examiner Thong Q. Le	Art Unit 2827	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,331,943	12-2001	Naji et al.	365/158
*	B	US-6,324,093	11-2001	Perner et al.	365/171
*	C	US-5,907,514	05-1999	Lee et al.	365/200
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
057454-0979	10/691,513
APPLICANT: Hideto HIDAKA	
FILING DATE: October 24, 2003	GROUP: 2827

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Codes (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
TL		US	2002/0009003 A1	01/24/2002	Hartmann	Corresponds to DE 100 34062 A1
TL		US	6,646,911 B2	11/11/2003	Hidaka	Corresponds to DE 102 28 560 A1
TL		US	5,751,627	05/12/1998	Ooishi	

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No
TL		WO 99/53499	10/21/1999	HONEYWELL, INC		X	
TL		EP 1 132 924 A2	10/11/2000	HEWLETT-PACKARD COMPANY, A DELAWARE CORPORATION		X	
TL		EP 1 253 651 A2	10/30/2002	KABUSHIKI KAISHA TOSHIBA TOKYO		X	
TL		DE 100 34062 A1	01/24/2002	INFINEON TECHNOLOGIES AG	Corresponds to USP 2002/0009003 A1		X
TL		EP 1 189 239 A2	09/14/2001	HEWLETT-PACKARD COMPANY		X	
TL		DE 102 28 560 A1	05/15/2003	MITSUBISHI DENKI K.K.	Corresponds to USP 6,646,911 B2		X
TL		WO 01/54279 A1	07/26/2001	PAGEANT TECHNOLOGIES		X	

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
TL		Scheuerlein, R., et al. "A 10ns read and write non-volatile memory array using a magnetic tunnel junction and FET switch in each cell" IEEE International Solid-State Circuits Conference, February 7-9, 2000, pp 128-129.
TL		Durlam, M., et al. "Nonvolatile RAM based on magnetic tunnel junction elements" IEEE International Solid-State Circuits Conference, February 7-9, 2000, pp 130-131.
TL		Naji, P., et al. "A 256kb 3.0V 1T1MTJ nonvolatile magnetoresistive RAM" IEEE International Solid-State Circuits Conference, February 7-9, 2001, pp 122-123, 438.
TL		Wee, J., et al. "An antifuse EPROM circuitry scheme for field-programmable repair in DRAM" IEEE Journal of Solid-State Circuits, Vol. 35, No. 10, October 2000, pp 1408-1414.
TL		Black, W., et al. "Programmable logic using giant-magnetoresistance and spin-dependent tunneling devices (invited)" Journal of Applied Physics, Vol. 87, No. 9, May 2000, pp 6647-6679.

EXAMINER	DATE CONSIDERED
Moyle	12/7/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 03/09/2005

McDermott, Will & Emery
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
LE, THONG QUOC	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/09/2005

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,513	10/24/2003	Hideto Hidaka	57454-979	7421

TITLE OF INVENTION: THIN FILM MAGNETIC MEMORY DEVICE FOR PROGRAMMING REQUIRED INFORMATION WITH AN ELEMENT SIMILAR TO A MEMORY CELL AND INFORMATION PROGRAMMING METHOD

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$1700	06/09/2005

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,513	10/24/2003	Hideto Hidaka	57454-979	7421

7590 03/09/2005

McDermott, Will & Emery
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/09/2005

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571) 272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

Notice of Allowability

Application No.	Applicant(s)	
10/691,513	HIDAKA, HIDETO	
Examiner	**Art Unit**	
Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.
2. ☒ The allowed claim(s) is/are *10-44*.
3. ☒ The drawings filed on *24 October 2003* are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☒ Certified copies of the priority documents have been received in Application No. *10/234,243* .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. Pre-amendment filed on January 07, 2005 has been entered.

2. Claims 10-44 are presented for examination.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 10/234,242, filed on 09/05/2002.

Reasons for Allowance

4. Claims 10-44 are allowed.

The following is an examiner's statement of reasons for allowance:

Claims 10-44 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Naji et al. (U.S. Patent No. 6,331,943) Perner et al. (U.S. Patent No. 6,324,093), Lee et al. (U.S. Patent No. 5,907,514), and others, does not teach the claimed invention having a thin film magnetic memory device comprises a program circuit for storing information for use in at least of data read operation and data write operation from and to the plurality of memory cells, wherein the program circuit includes a plurality of program units for storing program of information when the program unit is in a program state, and a redundant controller coupled to the address decoder and including a second memory for storing addresses of the defective normal memory cells of the first memory, wherein the second memory has a magneto-resistance element.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

THONG LE
PRIMARY EXAMINER

Applicant: Hideto HIDAKA Docket No. 57454-979

Title: THIN FILM MAGNETIC MEMORY DEVICE FOR PROGRAMMING REQUIRED INFORMATION WITH AN ELEMENT SIMILAR TO A MEMORY CELL AND INFORMATION PROGRAMMING METHOD Serial/Reg./Patent No. 10/691,513

Date Sent: 1/7/2005 ☒ Hand Carried ☐ Fax ☐ Electronic ☐ Cert. of Mailing ☐ First Class Mail ☐ Express Mail No. _____

☐ Transmittal Letter

New Patent App ☐ Utility ☐ Design ☐ Cont. ☐ CIP ☐ Div. ☐ PCT ☒ RCE ☐ Prov

☐ Other: _____

_____ pages of Specification

_____ pages of Claims

_____ pages of Abstract

_____ pages of Formal/Informal Drawings

☐ Small Entity ☐ Large Entity

☐ Declaration/Power of Attorney

☐ Recordation of Assignment/Security Agreement

☐ Information Disclosure Statement

_____ Form PTO 1449

_____ copies of cited references

☐ Preliminary Amendment

☐ Response to Missing Parts Notice

☐ Resp. to Notice to Correct App. Papers

☐ Certified Copy of Priority Doc.

☐ Claim for Convention Priority

☒ Response/Amendment to Notice of Allowance 10/8/04

☐ Request for _____ month Extension of Time

☐ Letter submitting _____ pages of drawings

☐ Req. for Approval of Drawing Amendments

☐ Req. for Oral Hearing

☐ Not. of Appeal ☐ Appeal Brief ☐ Reply Brief

☐ Rule 312 Amendment/Letter

☐ Req. for Acknowledgement of Cited Art

☐ Issue Fee

☐ Publication Fee

☐ Req. for Certificate of Correction

☐ Maintenance Fee for _____ years after grant

☐ Fee Address Indication Form

☐ Terminal Disclaimer

☐ Petition to Commissioner

☐ Status Inquiry

☐ Other _____

OIPE JC28
JAN 07 2005
PATENT & TRADEMARK OFFICE

Check for $		☒ Charge Deposit Acct. 500417$	1,040.00	Atty Init.	GZR	Tkpr. #	4234	Secy. or PL:	kkpollard

CMS Descrip.: (1) 790 (3) $250

THE PATENT AND TRADEMARK OFFICE DATE STAMPED HEREON IS ACKNOWLEDGEMENT THAT THE ITEMS, CHECKED ABOVE, WERE RECEIVED BY THE PTO ON THE DATE STAMPED.

OCT 31 2006

PTO/SB/30 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Request for Continued Examination (RCE) Transmittal

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	10/691,513
Filing Date	October 24, 2003
First Named Inventor	Hideto HIDAKA
Art Unit	2818
Examiner Name	LE, THONG
Attorney Docket Number	57454-979

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Education (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

   a. ☐ Previously submitted If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

      i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

      ii. ☐ Other _____

   b. ☒ Enclosed

      i. ☒ Amendment/Reply

      ii. ☐ Affidavit(s)/Declaration(s)

      iii. ☐ Information Disclosure Statement (IDS)

      iv. ☐ Other _____

2. Miscellaneous

   a. ☐ Suspension of action of the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

   b. ☐ Other _____

3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

   a. ☒ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 500417. I have enclosed a duplicate copy of this sheet.

      i. ☒ RCE fee required under 37 CFR 1.17(e) $790

      ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)

      iii. ☒ Other $250 (Additional Claims Fee)

   b. ☐ Check in the amount of $ _____ Enclosed

   c. ☐ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature	Gene Z. Rubinson	Date	January 7, 2005
Name (Print/Type)	Gene Z. Rubinson	Registration No.	33,351

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Signature			
Name(Print/Type)		Date	

Docket No.: 5[illegible]54-979 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Hideto HIDAKA	:	Confirmation Number: 7421
Application No.: 10/691,513	:	Group Art Unit: 2818
Filed: October 24, 2003	:	Examiner: LE, THONG Q.

For: THIN FILM MAGNETIC MEMORY DEVICE FOR PROGRAMMING REQUIRED INFORMATION WITH AN ELEMENT SIMILAR TO A MEMORY CELL AND INFORMATION PROGRAMMING METHOD

AMENDMENT UNDER 37 CFR 1.114

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The following Amendment and Remarks are submitted in response to the Notice of Allowance dated October 8, 2004 and are submitted pursuant to 37 C.F.R. § 1.114, together with a Request for Continued Examination (RCE) filed concurrently herewith.

AMENDMENTS TO THE CLAIMS

Claims 1-9 (cancelled)

10. (Previously Presented) A thin film magnetic memory device, comprising:

a memory array having a plurality of memory cells arranged in a matrix, for magnetically storing data, wherein

each of said memory cells has a magnetic storage portion for storing data when being magnetized in one of two directions,

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in at least one of data read operation and data write operation from and to said plurality of memory cells, wherein

said program circuit includes a plurality of program units for storing program data of said information when the program unit is in a program state,

each of said program units includes two program cells that are magnetized in one of two directions, and

when said program unit is in said program state, one of said two program cells in said program unit is magnetized in a direction different from that in a non-program state.

11. (Previously Presented) The thin film magnetic memory device according to claim 10, wherein

each of said magnetic storage portions and each of said program cells have a same structure,

when the program unit is in said non-program state, said two program cells in said program unit are magnetized in a same direction, and

a magnetization direction of said magnetic storage portions in an initial state is the same as that of said program cells in said non-program state.

12. (Previously Presented) The thin film magnetic memory device according to claim 10, wherein

the two magnetization directions of said magnetic storage portions and said program cells are respectively set along an easy axis specific to said magnetic storage portions and an easy axis specific to said program cells, and

said magnetic storage portions and said program cells are arranged so that said respective easy axes thereof extend in a same direction.

13. (Previously Presented) The thin film magnetic memory device according to claim 10, wherein

each of said magnetic storage portions and each of said program cells include

a first magnetic layer magnetized in a fixed direction,

a second magnetic layer magnetized either in a same direction as, or in an opposite direction to, that of said first magnetic layer depending on storage data, and

an insulating film formed between said first and second magnetic layers, and

in each of the program cells in said non-program state and each of the magnetic storage portions in said initial state, said first and second magnetic layers are magnetized in a same direction.

14. (Previously Presented) The thin film magnetic memory device according to claim 13, wherein a step of magnetizing said magnetic storage portions to said initial state and a step of said magnetizing each program cells to said non-program state are conducted simultaneously.

15. (Previously Presented) The thin film magnetic memory device according to claim 10, wherein

said memory array further includes

redundant circuits provided respectively corresponding to prescribed blocks of said plurality of memory cells, each for replacing the prescribed block including a defective memory cell, and

said information stored in said program circuit includes a defective address for specifying the prescribed block including said defective memory cell,

said thin film magnetic memory device further comprising:

a redundant control circuit for controlling access to said redundant circuits based on a comparison result between an address signal for selecting said prescribed blocks and said defective address stored in said program circuit.

16. (Previously Presented) The thin film magnetic memory device according to claim 15, wherein

when said defective address is selected by said address signal, said redundant control circuit provides an instruction to access said redundant circuits and an instruction to discontinue access to a prescribed block corresponding to said address signal.

17. (Previously Presented) The thin film magnetic memory device according to claim 15, further comprising:

a monitor terminal for outputting an electric signal according to said comparison result in said redundant control circuit.

18. (Previously Presented) The thin film magnetic memory device according to claim 10, wherein

each of said program cells has first and second electric resistances respectively corresponding to said two magnetization directions,

each of said program units further includes current sensing circuits provided respectively corresponding to said program cells,

in program data read operation from said program cells, each of said current sensing circuits applies a bias voltage to the corresponding program cell and outputs a binary voltage signal according to a current flowing through said corresponding program cell by said bias voltage,

each of said program units further includes a logic gate for outputting a first program signal, said first program signal indicating whether said program unit is in said program state or said non-program state according to a level of said binary voltage signal output from said current sensing circuits, and

each of said program units outputs one of said binary voltage signals respectively output from said current sensing circuits as a second program signal indicating a level of said program data.

19. (Previously Presented) The thin film magnetic memory device according to claim 18, wherein

each of said current sensing circuits applies said bias voltage to both a reference resistor having an electric resistance equal to an intermediate value of said first and second electric resistances and the corresponding program cell, and amplifies a difference between currents flowing through said reference resistor and said corresponding program cell and outputs said binary voltage signal.

20. (Previously Presented) The thin film magnetic memory device according to claim 10, wherein a bias voltage applied to each of said program cells in program data read operation from said program cells is lower than a voltage applied to each of said magnetic storage portions in normal data read operation.

21. (Previously Presented) The thin film magnetic memory device according to claim 10, wherein a period during which a bias voltage is applied to each of said program cells in program data read operation from said program cells is shorter than that during which a voltage is applied to each magnetic storage portion in normal data read operation.

22. (Previously Presented) The thin film magnetic memory device according to claim 10, wherein

in program data read operation, each program unit outputs a first program signal and a second program signal according to the magnetization directions of corresponding two program cells, said first program signal indicating whether said program unit is in said program state or said non-program state, and said second program signal indicating a level of said program data,

said program circuit further includes data latch circuits provided respectively corresponding to said program units, for holding said first and second program signals output from corresponding one of said program units,

said program data read operation is conducted in response to power-ON of said thin film magnetic memory device, and

said data latch circuits hold said first and second program signals from power-ON until power-OFF of said thin film magnetic memory device.

23. (Previously Presented) The thin film magnetic memory device according to claim 10, wherein

when the program unit is in said non-program state, said program cells in said program unit are magnetized in a same direction,

each program cell is magnetized by a first program magnetic field of a hard-axis direction and a second program magnetic field of an easy-axis direction,

said program circuit further includes

a program selection line shared by said two program cells of a same program unit, for receiving a first program current for generating said first program magnetic field, and

first and second program data lines provided respectively corresponding to said two program cells, for receiving a second program current for generating said second program magnetic field, and

said second program current is applied to said first and second program data lines in opposite directions.

24. (Previously Presented) The thin film magnetic memory device according to claim 23, wherein

said program circuit further includes

a voltage setting portion for connecting one end of said first program data line to one of first and second voltages and connecting one end of said second program data line to the other voltage according to a level of said program data, and

a program data line connection portion for electrically coupling the other ends of said first and second program data lines at least in said program data write operation.

25. (Previously Presented) The thin film magnetic memory device according to claim 23, wherein

each of said magnetic storage portions is magnetized by a first data write magnetic field of a hard-axis direction a second data write magnetic field of an easy-axis direction, and

each of said magnetic storage portions and each of said program cells have a same structure and same magnetic characteristics,

said thin film magnetic memory device further comprising:

a plurality of write selection lines provided respectively corresponding to memory cell rows, for receiving a first data write current for generating said first data write magnetic field in a selected row;

a plurality of write data lines provided respectively corresponding to memory cell columns, for receiving a second data write current for generating said second data write magnetic field in a selected column; and

a current supply circuit for supplying a prescribed current to a write selection line of said selected row as said first data write current, wherein

said current supply circuit supplies said prescribed current to said program selection line as said first program current in said program data write operation.

26. (Previously Presented) The thin film magnetic memory device according to claim 23, wherein

each of said magnetic storage portions is magnetized by a first data write magnetic field of a hard-axis direction a second data write magnetic field of an easy-axis direction, and

said magnetic storage portions and said program cells have a same structure and same magnetic characteristics,

said thin film magnetic memory device further comprising:

a plurality of write selection lines provided respectively corresponding to memory cell rows, for receiving a first data write current for generating said first data write magnetic field in a selected row;

a plurality of write data lines provided respectively corresponding to memory cell columns, for receiving a second data write current for generating said second data write magnetic field in a selected column; and

a current supply circuit for supplying a prescribed current to a write data line of said selected column as said second data write current, said prescribed current having a direction according to write data, wherein

said current supply circuit supplies said prescribed current to said program data lines as said second program current in said program data write operation.

27. (Previously Presented) The thin film magnetic memory device according to claim 10, wherein

each of said program cells includes a plurality of series-connected magneto-resistance elements, and

each of said magneto-resistance elements have a same structure and same magnetic characteristics as those of each of said magnetic storage portions.

28. (Previously Presented) A thin film magnetic memory device, comprising:

a memory array having a plurality of memory cells for magnetically storing data, wherein

each of said memory cells has a magnetic storage portion for storing data when being magnetized in one of two directions,

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in operation of said thin film magnetic memory device, wherein

said program circuit includes

a program element for magnetically storing program data of said information,

a sensing circuit for reading said program data from said program element in response to power-ON of said thin film magnetic memory device, and

a data latch circuit for holding said program data read by said sensing circuit until power-OFF of said thin film magnetic memory device.

29. (Previously Presented) A thin film magnetic memory device, comprising:

a memory array having a plurality of memory cells each magnetically storing one-bit data, wherein

each of said memory cells has a magneto-resistance element whose electric resistance varies when said magneto-resistance element is magnetized in a direction according to said data,

said thin film magnetic memory device further comprising:

a plurality of program registers each storing a one-bit program signal for use in programming of information used in operation of said thin film magnetic memory device, wherein

each program register includes

a plurality of program elements each having an electric resistance varying according to a magnetization direction thereof, and

a sensing circuit for reading a corresponding one-bit program signal according to a difference in electric resistance between said plurality of program elements, and

the number of said program elements included in each of said program registers is greater than that of said magneto-resistance elements used in each of said memory cells to store one-bit data.

30. (Previously Presented) The thin film magnetic memory device according to claim 29, wherein

each of said program elements and each of said magneto-resistance elements include

a first magnetic layer magnetized in a fixed direction,

a second magnetic layer magnetized either in a same direction as, or an opposite direction to, that of said first magnetic layer depending on said data and said program signal to be stored, respectively, and

an insulating film formed between said first and second magnetic layers, wherein

a difference between voltages applied to said first and second magnetic layers of each of said program elements upon reading said program signal is greater than that between voltages applied to said first and second magnetic layers of each of said magneto-resistance elements upon reading said data.

31. (Previously Presented) The thin film magnetic memory device according to claim 29, wherein

each pair of program registers forms a program unit for storing one-bit program data, and

said one-bit program signal stored in one program register of said pair of program registers indicates whether said program unit is in a non-program state or a program state.

32. (Previously Presented) A thin film magnetic memory device, comprising:

a memory array having a plurality of memory cells for magnetically storing data, wherein

each of said memory cells includes a magneto-resistance element having either a first electric resistance or a second electric resistance higher than said first electric resistance when being magnetized in a direction according to said data,

said thin film magnetic memory device further comprising:

a plurality of program registers each storing a one-bit program signal for use in programming of information used in operation of said thin film magnetic memory device, wherein

each of said program registers includes a plurality of program elements each having an electric resistance varying according to a magnetization direction thereof,

each of said program elements has either a third electric resistance lower than said first electric resistance or a fourth electric resistance higher than said third electric resistance according to said one-bit program signal stored therein, and

a ratio between said first and second electric resistances is equal to that between said third and fourth electric resistances.

33. (Previously Presented) The thin film magnetic memory device according to claim 32, wherein

each of said program elements and each of said magneto-resistance elements includes

a first magnetic layer magnetized in a fixed direction,

a second magnetic layer magnetized either in a same direction as, or an opposite direction to, that of said first magnetic layer depending on said data and said program signal to be stored, and

an insulating film formed between said first and second magnetic layers, wherein

a current passage area in said first and second magnetic layers and said insulating layer upon reading said program signal from each of said program elements is greater than that in said first and second magnetic layers and said insulating layer upon reading said data from each of said magneto-resistance elements.

34. (Previously Presented) A thin film magnetic memory device, comprising:

a memory array having a plurality of memory cells arranged in a matrix, for magnetically storing data, wherein

each of said memory cells has a magnetic storage portion for storing

data when being magnetized in one of two directions,

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in at least one of data read operation and data write operation from and to said plurality of memory cells, wherein

said program circuit includes a plurality of program units for storing program data of said information when the program unit is in a program state,

each of said program units includes at least one program cell that is magnetized for data writing, and

a magnetization direction of each said magnetic storage portion in an initial state is the same as that of each said program cell in a non-program state.

35. (Previously Presented) A thin film magnetic memory device, comprising:

a memory array having a plurality of memory cells arranged in a matrix, for magnetically storing data, wherein

each of said memory cells has a magnetic storage portion for storing

data when being magnetized in one of two directions,

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in at least one of data read operation and data write operation from and to said plurality of memory cells, wherein

said program circuit includes a plurality of program units for storing program data of said information when the program unit is in a program state,

each of said program units includes at least one program cell that is magnetized for data writing, and wherein

the magnetization directions of each said magnetic storage portion and each said program cell are respectively set along an easy axis specific to said program cell, and

said magnetic storage portion and said program cell are arranged so that said respective easy axis thereof extend in a same direction.

36. (Previously Presented) A thin film magnetic memory device, comprising:

a memory array having a plurality of memory cells arranged in a matrix, for magnetically storing data, wherein

each of said memory cells has a magnetic storage portion for storing data when being magnetized in one of two directions,

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in at least one of data read operation and data write operation from and to said plurality of memory cells, wherein

said program circuit includes a plurality of program units for storing program data of said information when the program unit is in a program state,

each of said program units includes at least one program cell that is magnetized for data writing, and wherein

each said magnetic storage portion and each said program cell include

a first magnetic layer magnetized in a fixed direction,

a second magnetic layer magnetized either in a same direction as, or in an opposite direction to, that of said first magnetic layer depending on storage data, and

an insulating film formed between said first and second magnetic layers, and

in each said program cell in said non program state and each said magnetic storage portion in said initial state, said first and second magnetic layers are magnetized in a same direction.

37. (Previously Presented) The thin film magnetic memory device according to claim 36, wherein a step of magnetizing said magnetic storage portions to said initial state and a step of said magnetizing each program cells to said non-program state are conducted simultaneously.

38. (Previously Presented) A thin film magnetic memory device, comprising: a memory array having a plurality of memory cells arranged in a matrix, for magnetically storing data, wherein

each of said memory cells has a magnetic storage portion for storing data when being magnetized in one of two directions,

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in at least one of data read operation and data write operation from and to said plurality of memory cells, wherein

said program circuit includes a plurality of program units for storing program data of said information when the program unit is in a program state,

each of said program units includes at least one program cell that is magnetized for data writing, and wherein

said memory array further includes

redundant circuits provided respectively corresponding to prescribed blocks of said plurality of memory cells, each for replacing the prescribed block including a defective memory cell, and

said information stored in said program circuit includes a defective address for specifying the prescribed block including said defective memory cell,

said thin film magnetic memory device further comprising:

a redundant control circuit for controlling access to said redundant circuits based on a comparison result between an address signal for selecting said prescribed blocks and said defective address stored in said program circuit.

39. (Previously Presented) The thin film magnetic memory device according to claim 38, wherein

when said defective address is selected by said address signal, said redundant control circuit provides an instruction to access said redundant circuits and an instruction to discontinue access to a prescribed block corresponding to said address signal.

40. (Previously Presented) The thin film magnetic memory device according to claim 38, further comprising:

a monitor terminal for outputting an electric signal according to said comparison result in said redundant control circuit.

41. (Previously Presented) A thin film magnetic memory device, comprising: a memory array having a plurality of memory cells arranged in a matrix, for magnetically storing data, wherein

each of said memory cells has a magnetic storage portion for storing data when being magnetized in one of two directions,

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in at least one of data read operation and data write operation from and to said plurality of memory cells, wherein

said program circuit includes a plurality of program units for storing program data of said information when the program unit is in a program state,

each of said program units includes at least one program cell that is magnetized for data writing, and wherein

a bias voltage applied to each said program cell in program data read operation from said program cell is lower than a voltage applied to each said magnetic storage portion in normal data read operation.

42. (Previously Presented) A thin film magnetic memory device, comprising:

a memory array having a plurality of memory cells arranged in a matrix, for magnetically storing data, wherein

each of said memory cells has a magnetic storage portion for storing data when being magnetized in one of two directions,

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in at least one of

data read operation and data write operation from and to said plurality of

memory cells, wherein

said program circuit includes a plurality of program units for storing program data of said information when the program unit is in a program state,

each of said program units includes at least one program cell that is magnetized for data writing, and wherein

a period during which a bias voltage is applied to each said program cell in program data read operation from said program cell is shorter than that during which a voltage is applied to each said magnetic storage portion in normal data read operation.

43. (Previously Presented) A thin film magnetic memory device, comprising:

a memory array having a plurality of memory cells arranged in a matrix, for magnetically storing data, wherein

each of said memory cells has a magnetic storage portion for storing data when being magnetized in one of two directions,

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in at least one of data read operation and data write operation from and to said plurality of memory cells, wherein

said program circuit includes a plurality of program units for storing program data of said information when the program unit is in a program state,

each of said program units includes at least one program cell that is magnetized for data writing, and wherein

a voltage supplied to each said program cell in program data operation by a physical breakdown operation is higher than a voltage applied to each said magnetic storage portion in normal data read operation.

44. (New) A semiconductor memory device, comprising:

a first memory including normal memory cells for storing data therein;

an address decoder coupled to said first memory and selecting the normal memory cells according to the address provided to the semiconductor memory device; and

a redundant controller coupled to said address decoder and including a second memory for storing addresses of the defective normal memory cells of said first memory, wherein said second memory has a magneto-resistance element;

said semiconductor memory device further comprises

a third memory including spare memory cells for repairing the defective normal memory cells; and

a redundant address decoder coupled to said redundant controller and said third memory, and selecting the spare memory cells according to the address stored in said second memory.

REMARKS

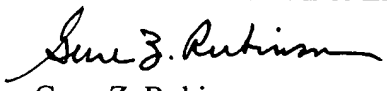
Claims 10 through 44 are pending in this application. Applicants acknowledge, with appreciation, the Examiner's allowance of claims 10 through 43. New claim 44 has been added. Care has been exercised to avoid the introduction of new matter. Applicant submits that the present Amendment does not generate any new matter issue.

Favorable consideration of new claim 44 is requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Gene Z. Rubinson
Registration No. 33,351

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 GZR:kap
Facsimile: 202.756.8087
Date: January 7, 2005

Please recognize our Customer No. 20277 as our correspondence address.